EE 209 Spiral 1 Exam
Solutions

Name: _____

1.) Answer the following questions as True or False

a.) *A 4-to-1 multiplexer requires at least 4* ***select*** *lines*: **true / false**

FALSE

b.) *An 8-to-1 mux and no other logic can be used to implement any combinational logic function of 4 input variables*: **true / false**

FALSE

c.) *A 3-to-8 decoder along with (4) 8-input OR gates can be used to implement any combinational logic involving 3 input variables and 4 output variables*: **true / false**

TRUE

d.) *3 separate 2-to-1 muxes can be used to build a single 4-to-1 mux*: **true / false**

TRUE

e.) *5 flip-flops are required to implement a state machine with 5 states*: **true / false**

FALSE

f.) *In a state machine with Moore style outputs, a change in the external inputs can independently and immediately cause the outputs to change*: **true / false**

FALSE

g.) What are the three primary design goals that we try to optimize in circuit design?

1.) Area or Size 2.) Speed or Delay 3.) Power

h.) Given a 5-to-32 decoder with inputs (A4, A3, A2, A1, A0), write out the logic equation for output 17 (i.e. O17)?

17 10001_2 = A4 •A3' •A2' •A1' •A0

i.) A 20-to-1 mux would require a minimum of how many select bits?

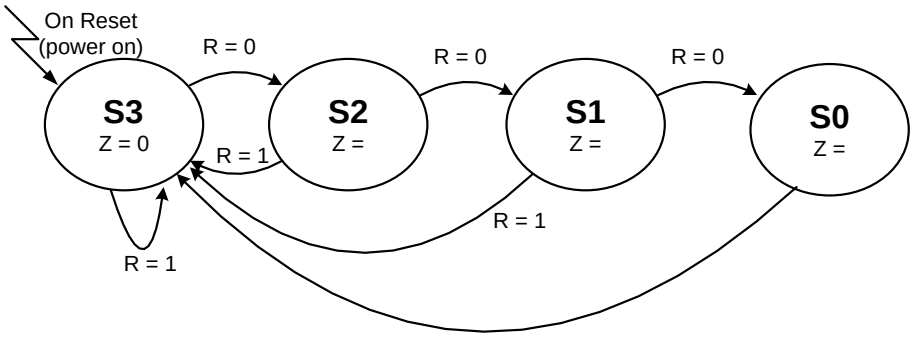
5 bits

2.) **State Machine Design (Down Counter w/ Restart)**: Design a synchronous state machine circuit that implements a 2-bit down counter (i.e. counts 11, 10, 01, 00, 11…). The circuit has an external input, R (RESTART), that when '1' should force the counter back to the 11 state no matter what the current state is. As long as R stays '1', the counter should stay in the 11 state. The circuit should also have one output Z. Z=1 when in the 00 state and Z = 0 otherwise.

Let us use 4 states:

S3 (initial state on reset)	The count should be $11_2 = 3_{10}$
S2	The count should be $10_2 = 2_{10}$
S1	The count should be $01_2 = 1_{10}$
S0	The count should be $00_2 = 0_{10}$

a.) Complete the state diagram below by filling in all necessary transitions **and** the values of Z.



b.) What is the minimum number of flip-flops required to implement this state machine?

2 Flip Flops

c.) Complete the state transition/output table given below. (Note: We have provided the state assignment already). We have ordered the states in such a way to use gray code ordering, so take care when translating your state diagram to the transition/output table.

Current State		Next State				Output
		R=0		R=1		
State	Q_1Q_0	State	$Q_1^*Q_0^*$	State	$Q_1^*Q_0^*$	Z
S0	0 0	S3	1 1	S3	1 1	1
S1	0 1	S0	0 0	S3	1 1	0
S3	1 1	S2	1 0	S3	1 1	0
S2	1 0	S1	0 1	S3	1 1	0

d.) Assume we will implement our circuit using D Flip-Flops. Use the K-Maps below to find minimal expressions for D1, D0, and Z.

D_1 Map

Q_1Q_0 \ R	0	1
00	1	1
01	0	1
11	1	1
10	0	1

$D_1 = R + Q1'Q0' + Q1Q0$

D_0 Map

Q_1Q_0 \ R	0	1
00	1	1
01	0	1
11	0	1
10	1	1

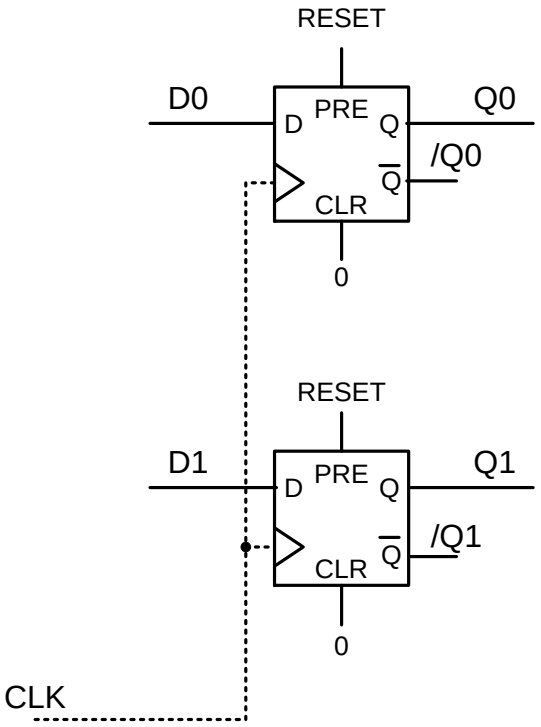
$D_0 = R + Q0'$

Z Map

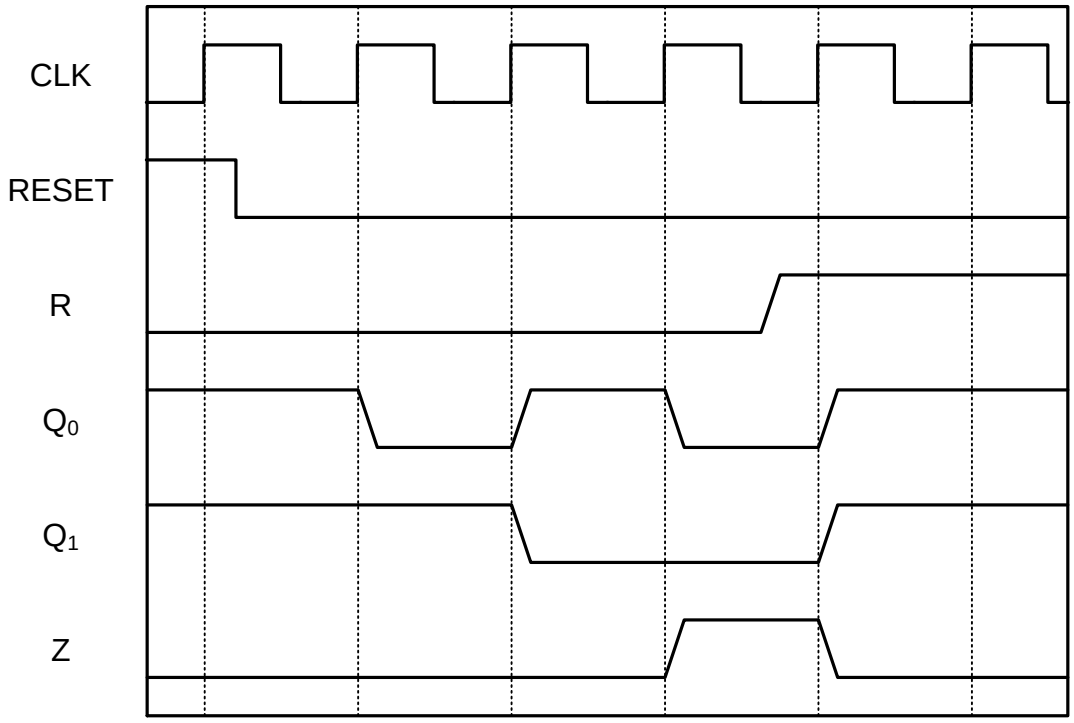
Q_0 \ Q_1	0	1
0	0: 1	2: 0
1	1: 0	3: 0

$Z = Q1'Q0'$

e.) Show how to implement the initial state (power-on/reset state) by connecting the PRE (PRESET) and CLR inputs of the FF's appropriately. Assume the signal RESET is available to you. You do not need to implement the next-state or output-function logic.



f.) Using your design above draw the waveform for the sequence of states that the machine will go through and what the output will be for the given input sequence of X. Remember you are using positive edge-triggered devices.



3. Find the simplest SOP form of the following logic equation.

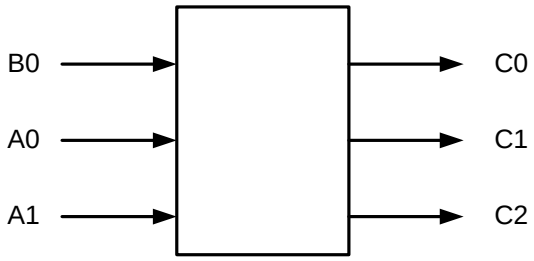
$$F = \overline{[(\overline{A}+C)\bullet\overline{B}+(\overline{A}+C)\bullet\overline{C}]}+AB\overline{C}$$

F	= ((AC')+B)((AC')+C) + ABC'	DeMorgan's
	= AC' + BC + ABC'	T8'
	= AC' + BC	T9

Single-Variable Theorems				
(T1)	X + 0 = X	(T1')	X • 1 = X	(Identities)
(T2)	X + 1 = 1	(T2')	X • 0 = 0	(Null elements)
(T3)	X + X = X	(T3')	X • X = X	(Idempotency)
(T4)	(X')' = X			(Involution)
(T5)	X + X' = 1	(T5')	X • X' = 0	(Complement)
Two- and Three-Variable Theorems				
(T6)	X +Y = Y + X	(T6')	X • Y = Y • X	(Commutativity)
(T7)	(X+Y)+Z = X+(Y+Z)	(T7')	(X•Y) •Z = X• (Y•Z)	(Associativity)
(T8)	X•(Y+Z) = X•Y + X•Z	(T8')	X+(Y•Z) = (X+Y) • (X+Z)	(Distributivity)
(T9)	X + X•Y = X	(T9')	X • (X + Y) = X	(Covering)
(T10)	X•Y + X•Y' = X	(T10')	(X+Y) • (X+Y') = X	(Combining)
(T11)	X•Y+X'•Z+Y•Z = X•Y+X'Z	(T11')	(X+Y)•(X'+Z)•(Y+Z) = (X+Y)•(X'+Z)	(Consensus)
DeMorgan's Theorem				
	(X • Y)' = X' + Y'	(T6')	(X +Y)' = X' • Y'	(DeMorgan's)

4. Design a circuit takes a 2-bit, **unsigned** number **A=**(A_1A_0) and a 1-bit, **unsigned** number **B**=(B_0) as input and produces the output **C** = A – B represented in the **2's complement system**. (25 pts.)

a.) Complete the block diagram of this circuit by showing and labeling the inputs and outputs. Think how many output bits are required. (2 pts.)



b.) Write out a truth table for this circuit. (8 pts.)

A1	A0	B0	C2	C1	C0
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	0	1	1
1	1	1	0	1	0

c.) Find the minimal **SOP** expression for each bit of output by using the 3 K-Maps furnished below. Make sure to add the variable labels for the axes of each K-Map and add your gray code. **Clearly indicate** the minimal expressions you find for each output. (12 pts.)

B_0 \ A_1A_0	00	01	11	10
0	0	0	0	0
1	1	0	0	0

$C_2 = A_1'A_0'B_0$

B_0 \ A_1A_0	00	01	11	10
0	0	0	1	1
1	1	0	1	0

$C_1 = A_1'A_0'B_0 + A_1A_0 + A_1B_0'$

B_0 \ A_1A_0	00	01	11	10
0	0	1	1	0
1	1	0	0	1

$C_2 = A_0B_0' + A_0'B_0$

5.) Complete the waveform for the given circuit