SYLLABUS

Foundations of Digital System Design

EE 209: Fall 2017 (4 units)

This course introduces digital system design theory and practice. It focuses on logic design techniques and physical implementation methodologies. Students learn to design and synthesize combinational and sequential logic structures at the gate and transistor level using structures and concepts learned in EE 109L. Topics include Boolean algebra, datapath components, state machine synthesis, implementation technologies with focus on CMOS, and physical layout. A lab component familiarizes students with standard electronic design automation (EDA) software tools with implementation to FPGAs to allow students to put theory into practice.

Instructor: Brandon Franzke
Email: franzke@usc.edu
Office: EEB 420

Hours: Monday 09:00 – 10:30
Tuesday 09:30 – 11:00
Wednesday afternoon (by appointment)

Lecture

Monday and Wednesday (section: 30773)
10:30 – 12:00

Tuesday and Thursday (section: 30777)
11:00 – 12:30

Piazza

Piazza is suited to getting you help fast and efficiently from classmates, the TAs, and myself. I encourage you to post your questions on Piazza rather than emailing questions to the teaching staff.

Class page: https://piazza.com/usc/fall2017/ee209/home

TAs and grader

The TAs lead lab discussions and are valuable resources to help you with challenging course material. You may approach any TA with questions pertaining to EE 209.

TA: Rebecca Lee
Office: VHE 205
Office hours: Tuesday 17:00 – 18:00
Thursday 17:00 – 19:00
Email: leerk@usc.edu
Grader: Divya Nandihalli
Office hours: by appointment
E-mail: nandihal@usc.edu

TA: Chao (Albert) Wang
Office: VHE 205
Office hours: Monday 15:30 – 16:00
Thursday 12:30 – 14:00
Email: wang484@usc.edu

Course materials

Online content (Blackboard): http://blackboard.usc.edu
References (Required): "Digital Design with RTL Design, Verilog and VHDL", 2nd edition, Frank Vahid, 2010, (ISBN: 0470531088).

Learning Objectives

Upon completion of this course students will be able to:

1. Identify and derive appropriate logic functions to implement a specified design
2. Synthesize logic circuits to implement a given logic function
3. Understand design tradeoffs that include area and speed and optimize circuits for desired performance
4. Analyze and manipulate logic circuits to ascertain their logic function or alter their implementation based on specific design requirements
5. Synthesize and analyze circuits that include state elements (flip-flops) [i.e. state machines]
6. Design datapath and control units for portions of a simple CPU
7. Understand basic principles of semiconductor physics and transistor operation
8. Layout simple logic cells
9. Understand the relationship of delay and area due to the parasitics inherent in physical implementation.

Grading Procedure

Homework

Assigned approximately bi-weekly. Homework is meant to supplement topics that we might not cover fully in class. Staying current with the class requires practice to master the concepts. Experience has shown that students who put in the effort on these homeworks, struggle with problems, and ask questions when they did not understand a problem did the best in this course.

The total homework score sums your best homework scores (as a percentage) after removing the lowest score. Homeworks with Blackboard submissions are due by the date and time posted. Homeworks with hard copy submissions are due by **18:00 on the posted due date to the EE209 HW locker** in the basement of EEB near room B24. **All circuit drawings should be neatly in Xilinx**. Late homework will be accepted with a **20% deduction per day for up to 2 days only if the solutions are not distributed**. Late homework can be submitted by placing it in the EE209 HW locker and sending an email to me **and copying the grader**. Homework will not be accepted after solutions are distributed. Solutions are usually posted 2 days after the due date. If you cannot make it to a lecture you may turn your homework in early or ask a friend to turn it in for you.

Students may discuss homework problems among themselves but each student must do his or her own work. Cheating warrants an F in the course. Turning in identical homework sets counts as cheating.

Discussion/Lab

Lab exercises will consist of small logic designs using a digital training board, FPGA boards, and logic simulators. These lab exercises are meant to give students an opportunity to work with actual hardware and provide concrete examples to the pencil and paper designs discussed in lecture. FPGA boards will be available in lab and during TA office hours. Labs must be checked off **at the beginning of your discussion section** and submitted online as well immediately after being demoed. Late submissions must demonstrate and submit code by the next discussion following the due date.

Exams

All exams will be closed book. The course has two two-hour exams and two fifty-minute checkpoint quizzes. The exams will be held during the Quiz section (which is the only time we will use that slot). There are no calculators allowed, only pen or pencils and an eraser. You must show how you arrived at your answers to receive full credit. Any cheating may result in an “F” in the course and will be referred to Student Affairs for other penalties. Make up exams will only be given for valid medical or family emergency excuses (proof required).

Course Grade

HW	10% (lowest thrown out)	A	if 90 – 100 points
Quizzes	20%	B	if 80 – 89 points
Exam 1	15%	C	if 70 – 79 points
Exam 2	20%	D	if 60 – 69 points
Labs	35%	F	if 0 – 59 points
		("+" and "-" within approx. 3% of grade boundary)	

Attendance and Participation

Attendance is mandatory to all lectures and discussions. You are responsible for missed announcements or changes to the course schedule or assignments.

Cheating

Cheating is not tolerated on homework or exams. Penalty ranges from F on exam to F in course to recommended expulsion.

Course Outline (tentative)

21 Aug	Course overview
23 Aug	Combinational vs. sequential, clocking methodologies, design goals, logic functions
28 Aug	Single variable Boolean algebra, decoders, muxes
30 Aug	Minterms and maxterms, canonical sums, synthesis using Boolean algebra, structural Verilog
04 Sep	**No class: Labor Day, University holiday**
06 Sep	Synthesis using Karnaugh maps
11 Sep	Karnaugh maps (cont.), registers, state machines design overview
13 Sep	State machine design
13 Sep	**Quiz 1, 19:00 – 20:00**
18 Sep	State machine design (cont.)
20 Sep	Transistor switching models, nMOS, pMOS, and CMOS.
25 Sep	CMOS (cont.), fabrication process overview
27 Sep	Datapath components (adders and counters)
02 Oct	Memories + Midterm Review
04 Oct	Datapath components (fast adders, comparators, memories)
04 Oct	**Exam 1, 19:00 – 21:00**
09 Oct	Negative logic, one-hot state machine design, multiplier system design example
11 Oct	Multiplier & vending machine system design examples
16 Oct	System design (cont.)
18 Oct	Combinational synthesis using muxes & memories
23 Oct	Sequential components (bistable gates, latches, and FFs)
25 Oct	MOS theory
25 Oct	**Quiz 2, 19:00 – 20:00**
30 Oct	Capacitance, delay, and sizing
01 Nov	capacitance and delay (cont.)
06 Nov	Layout + memory cells, sequential components
08 Nov	memory cells (cont.)
13 Nov	ASIC vs. FPGA, hardware/software interfacing, PicoBlaze

15 Nov	Project overview, interfacing (cont.)
20 Nov	examples
22 Nov	**No class: Thanksgiving, University holiday**
27 Nov	Single-cycle CPU
29 Nov	No class
29 Nov	**Exam 2, 19:00 – 21:00**

Academic Conduct

Academic Integrity

Academic integrity is critical the assessment and evaluation we perform which leads to your grade. In general, all work should be your own and any sources used should be cited. Gray-areas occur when working in groups. Telling someone how to do the problem or showing your solution is a VIOLATION. Reviewing examples from class or other sources to help a fellow classmate understand a principle is fine and encouraged. All students are expected to understand and abide by these principles. SCampus, the Student Guidebook, contains the University Student Conduct Code in Section 10, while the recommended sanctions are located in Appendix A. Students will be referred to the Office of Student Judicial Affairs and Community Standards for further review, should there be any suspicion of academic dishonesty.

Plagiarism

Presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in SCampus in Section 11, Behavior Violating University Standards https://scampus.usc.edu/1100-behavior-violating-university-standards-andappropriate-sanctions. Other forms of academic dishonesty are equally unacceptable. See additional information in SCampus and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct.

Support Systems

Discrimination, sexual assault, and harassment are not tolerated by the university. You are encouraged to report any incidents to the Office of Equity and Diversity http://equity.usc.edu or to the Department of Public Safety http://capsnet.usc.edu/department/department-public-safety/online-forms/contactus. This is important for the safety of the whole USC community. Another member of the university community – such as a friend, classmate, advisor, or faculty member – can help initiate the report, or can initiate the report on behalf of another person. The Center for Women and Men http://www.usc.edu/studentaffairs/cwm/ provides 24/7 confidential support, and the sexual assault resource center webpage http://sarc.usc.edu describes reporting options and other resources.

Academic Accommodations

Any student requiring academic accommodations based on a disability is required to register with Disability Services and Programs (DSP) each semester. A letter of verification for approved accommodations can be obtained from DSP. Please be sure the letter is delivered to me as early in the semester as possible. DSP is located in GFS 120 and is open 08:30 – 17:00, Monday through Friday. The phone number for DSP is (213) 740-0776.

Emergency Preparedness/Course Continuity in a Crisis

In case of a declared emergency if travel to campus is not feasible, USC executive leadership will announce an electronic way for instructors to teach students in their residence halls or homes using a combination of Blackboard, teleconferencing, and other technologies.